REMARKS

Claims 1-25 remain in this application. The Office Action has indicated that claims 2-6, 11-18 and 20-25 are allowed.

REJECTIONS TO THE CLAIMS UNDER 35 U.S.C. § 103(a)

Claims 1, 7-10, and 19 were rejected under 35 U.S.C. § 102(b) as being anticipated U.S. Patent No. 5,034,744 to Obinata ("Obinata"). Claims 8-9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Obinata.

In the Response to Arguments section, the Examiner states that "the current claim language does not define or require any particular structure or component for detecting the sample bit having one logic value and adjacent bits on both sides of [the] sample bit having one logic value and adjacent bits on both sides of [the] sample bit each having an opposite logic value to the one logic value of [the] sample bit. Therefore any reference discloses a method of detecting and suppression [of] a single bit as glitch, that reference would either inherently or expressively disclose the step of detecting a sample bit having one logic value and adjacent bits on both sides of [the] sample bit each having an opposite logic value to the one logic value of [the] sample bit. Without detecting the both [sides] of [the] glitch, there is no way of telling whether the bit is a glitch or a correct bit. In addition, the reference clearly discloses that after a glitch is detected, it will be deglitched accordingly (e.g., col. 2, lines 36-63)."

The cited section of Obinata is the Summary of the Invention section and includes "objects of the invention." The Summary refers to the circuit described in the Detailed

Description section of the patent. The claim language of the independent claims refers to "detecting a sample bit having one logic value and adjacent bits on both sides of said sample bit each having an opposite logic value to the one logic value of said sample bit" and "outputting the received word with the sample bit having said one logic value inverted." (e.g., claim 1). If such language reads on any structure or component, then for a reference to be a proper reference under 35 U.S.C. § 102 it must teach such a detection, or such must be inherent from it. Neither is true with Obinata.

As detailed in the previous Office Action Response, a glitch in Obinata is detected when a sample bit is different than the previous sample bit. There is no disclosure, inherent or otherwise for determining whether adjacent bits on both sides of a sample bit have an opposite logic value than that of the sample bit. Looking at Fig. 1, the comparison that is taking place at the output of the D-type flip-flops 30-33 is the comparison of the current bit (input to the flip flop) with the previous bit (output of the flip-flop). That is the explicit disclosure of the reference. There is nothing inherent in Obinata that even remotely suggests that both bits adjacent to the sample bit are being compared to the logic value of the sample bit.

The Office Action states that "without detecting the both side of glitch, there is no way of telling whether the bit is a glitch or a correct bit." That statement is not supported by the specification of Obinata. Col. 3, lines 14-57 describes the type of glitch that is the focus of the circuit of Fig. 1. As seen from Fig. 1, the indication of whether there is a difference between a current bit and a previous bit is shown by the outputs of XOR gates 34-37, the combinatorial logic to the right of the XOR gates. The output of NAND gate 39 becomes low only with the

second most significant bit changes value without the most significant bit changing its value (see Col. 3, lines 58-62). The other gates are making similar types of comparisons to provide a positive or negative deglitching pulse (see Col. 5, line 57 to Col. 6, line 2). See also Fig. 2a, which shows the comparison of eight bit values (i.e., the outputs of element 23 and the outputs of flip-flops 30-33).

The feature of independent claims 1, 10 and 19 is neither shown, explicitly or inherently, by Obinata and is not obvious in view of Obinata disclosure of correcting a particular type of glitch found in a Philips TDA 1541S1 DAC. Accordingly, reconsideration and withdrawal of the rejections of the claims under 35 U.S.C. §§ 102(b) and 103(a) is respectfully requested.

CONCLUSION

For all the above reasons, the Applicant respectfully submits that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (202) 220-4200 to discuss any matter concerning this application. The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. § 1.16 or § 1.17 to Deposit Account No. 11-0600.

Respectfully submitted,
KENYON & KENYON LLP

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By: _____
Shawn W. O'Dowd
Reg. No. 34,687

KENYON & KENYON LLP
1500 K Street, NW
Suite 700
Washington, DC 20005
(202) 220-4200 telephone
(202) 220-4201 facsimile
DC-641073